IN THE SPECIFICATION

Please amend the Abstract as follows:

-- A data transceiver including a self-test data generator for generating test data, which includes a first pseudo-random number generator ~~capable of generating a digital word. The first pseudo-random number generator is also~~ programmable so as to allow the operator to input the test data values. The data transceiver further includes a transmitter section coupled to the self-test data generator, ~~which is operable for receiving the test data and processing the test data in the same manner as any other data to be transmitted by the transmitter section. The data transceiver also includes~~ a receiver section coupled to the transmitter section, and ~~which is operable for receiving the test data output by the transmitter section and for processing the test data in the same manner as any other data to be received by the receiver section. The data transceiver also includes~~ a test data analyzer coupled to the receiver section, wherein the ~~which is operative for verifying the accuracy of the test data output by the receiver section, and outputting an error signal if there is an error in the test data. The~~ test data analyzer includes a second pseudo-random number generator ~~capable of generating a digital word~~, which allows the operator to input the data value via a data bus coupled to the test data analyzer. Both the self-test data generator and the test data analyzer are independently controllable.--

Please replace the following paragraph beginning at page 13, line 18 and ending at page 14, line 2 with the following rewritten paragraph:

-- In the preferred embodiment, the BIST analyzer circuit 49 [[19]] comprises a comparator capable of comparing the two 16 bit data words. Each clock cycle the comparator functions to compare the data signal generated internally by the pseudo random signal generator and the data signal retrieved from the holding register 48. However, it is noted that there are numerous

acceptable variations for implementing the BIST analyzer circuit 49, and the present invention should not be construed so as to be limited to the embodiment disclosed above.--